Amendments to the Claims

This listing claims will replace all prior versions, and listings of claims in this application:

Listing of claims:

Claims 1-21 (Canceled)

Claim 22 (Previously Presented): An apparatus for down scaling a plurality of input frames to output a plurality of output frames, comprising:

a data buffer, for buffering the input frames and outputting the output frames according to a decision signal; and

a down-scaling control circuit, coupled to the data buffer, for generating the decision signal according to a scaling ratio parameter, the down-scaling control circuit comprising:

a selector for selecting a plurality of first sampling positions in a first input frame, a plurality of first skipping positions in the first input frame, a plurality of second sampling positions in a second input frame, and a plurality of second skipping positions in the second input frame according to the scaling ratio parameter; and outputting a selection signal; and

a control logic, for outputting the decision signal according to the selection signal;

wherein at least one of the second sampling positions in the second input frame is corresponding to one of the first skipping positions in the first input frame; and at least one of the first sampling positions in the first input frame is corresponding to one of the second skipping positions in the second input frame.

Claim 23 (Previously Presented): The apparatus of claim 22, wherein the selector further comprises:

a horizontal pixel selector for selecting a plurality of first sampling pixel positions of each horizontal line of the first input frame and a plurality of second sampling pixel positions of each horizontal line of the second input frame; and

a horizontal line selector for selecting a plurality of first sampling horizontal line positions of the first input frame and a plurality of second sampling horizontal line positions of the second input frame.

Claim 24 (Previously Presented): The apparatus of claim 22, wherein the down-scaling control circuit further comprises:

an odd/even decision unit, for determining whether the input frames is an odd frame or an even frame according to a vertical synchronization signal.

Claim 25 (Previously Presented): The apparatus of claim 22, wherein the control logic is an AND gate.

Claim 26 (New) The apparatus of claim 22, wherein the selector selects the first sampling positions in the first input frame, the second sampling positions input frame according to a first offset value and second offset value respectively.

Claim 27 (New) The apparatus of claim 26, wherein when the first offset value is 0, the second offset value is M/N-1; wherein M is the number of horizontal pixels of the input frame, and N is the number of horizontal pixels of the output frame.

Claim 28 (New) The apparatus of claim 22, wherein the data buffer is a FIFO-type data buffer.